WHAT IS CLAIMED IS:

1	1. A fabrication method of forming a trenched DMOS device and a
2	termination structure thereof, the method comprising:
3	forming an N- epitaxial layer on an N+ silicon substrate;
4	forming an oxide layer on the N- epitaxial layer;
5	patterning the oxide layer to form a termination oxide layer therein to define
6	an exposed active area of the DMOS device;
7	implanting P-type ions into the active area by using the termination oxide
8	layer as a mask to form a P body in the N- epitaxial layer;
9	recessing the N- epitaxial layer to form a plurality of DMOS trenches in the
10	body by patterning and etching, the DMOS trenches having bottoms which extend beneath a
11	bottom of the P body;
12	forming a gate oxide layer over exposed surfaces of the P body;
13	depositing a polysilicon layer over exposed surfaces and also filling the
14	DMOS trenches;
15	recessing the polysilicon layer to form a plurality of polysilicon gates and a
16	polysilicon plate by patterning and etching, wherein the polysilicon gates are positioned in
17	the DMOS trenches and the polysilicon plate is positioned over the termination oxide layer
18	and a portion of the gate oxide layer disposed adjacent the termination oxide layer;
19	implanting N-type ions into the P body by using the polysilicon plate and the
20	termination oxide layer as a mask to form a plurality of N+ diffused regions;
21	forming an isolation layer over exposed surfaces after implanting the N-type
22	ions;
23	patterning and anisotropically etching the isolation layer and the gate oxide
24	layer to form a plurality of body contact windows over the N+ diffused regions, and a first
25	contact window over the polysilicon plate;
26	implanting P-type ions through the body contact windows to form a plurality
27	of P+ diffused regions; and
28	forming a source metal contact layer disposed over the isolation layer, and
29	filling the body contact windows and the first contact window.
1	2. The method of claim 1, wherein the oxide layer on the N- epitaxial
2	layer is formed by thermal oxidation.

1	3. The method of claim 1, wherein the gate oxide layer is formed over the
2	exposed surfaces of the P body by thermal oxidation.
1	4. The method of claim 1, further comprising forming a drain metal
2	contact layer on a back surface of the N+ silicon substrate.
1	5. The method of claim 4, further comprising removing unnecessary
2	layers formed on the back surface of the N+ silicon substrate prior to forming the drain metal
3	contact layer.
1	6. The method of claim 5, wherein the unnecessary layers formed o the
2	back surface of the N+ silicon substrate are removed by chemical mechanical polishing.
1	7. The method of claim 1, further comprising forming a sacrificial oxide
2	layer on the active area after forming the termination oxide layer.
1	8. The method of claim 6, further comprising removing the sacrificial
2	oxide layer by etching after forming the DMOS trenches but before forming the gate oxide
3	layer.
1	9. The method of claim 1, wherein the polysilicon plate comprises a
2	portion extending toward one of the DMOS trenches disposed closest to the polysilicon plate
1	10. The method of claim 1, wherein anisotropically etching the isolation
2	layer to form the body contact windows and the first contact window includes a two-step
3	etching process which comprises:
4	removing portions of the isolation layer and the gate oxide layer by etching to
5	form the body contact windows and the first contact window; and
6	removing an exposed portion of the polysilicon plate at the first contact
7	window, and removing an exposed portion of the N+ diffused regions at the body contact
8	windows.
1	11. The method of claim 1, wherein patterning and anisotropically etching
2	to form the body contact windows and the first contact window comprises removing the
3	isolation layer and the gate oxide layer by etching while using the polysilicon plate and the

N+ diffused regions as etch stop layers.

1	12. The method of claim 1, wherein implanting P-type ions through the
2	body contact windows to form the plurality of P+ diffused regions comprises providing a
3	sufficient dose of the P-type ions to change an electric polarity of the N+ diffused region
4	exposed by the body contact windows to the P+ diffused regions.
1	13. The method of claim 1, wherein the isolation layer comprises doped
2	silicate glass.
1	14. The method of claim 1, wherein the source metal contact layer
2	comprises a stack of Ti, TiN, and AlSiCu alloy layers.
1	15. A method of forming a trenched DMOS device and a termination
2	structure thereof, the method comprising:
3	providing an N+ silicon substrate, an N- epitaxial layer on the N+ silicon
4	substrate, a termination oxide layer on the N- epitaxial layer, a P body in the N- epitaxial
5	layer, a plurality of DMOS trenches extending through the P body into the N-epitaxial layer,
6	and a gate oxide layer over exposed surfaces of the P body;
7	forming a trenched DMOS device having a plurality of polysilicon gates
8	disposed in the DMOS trenches, and a polysilicon plate disposed over the termination oxide
9	layer and over a portion of the gate oxide layer disposed adjacent the termination oxide layer
10	implanting N-type ions into a portion of the P body not covered by the
11	polysilicon plate and termination oxide layer to form a plurality of N+ diffused regions;
12	forming an isolation layer over exposed surfaces after implanting the N-type
13	ions;
14	patterning and etching the isolation layer and the gate oxide layer to form a
15	plurality of body contact windows over the N+ diffused regions, and a first contact window
16	over the polysilicon plate;
17	implanting P-type ions through the body contact windows to form a plurality
18	of P+ diffused regions; and
19	forming a source metal contact layer over the isolation layer, and filling the
20	body contact windows and the first contact window.

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The method of claim 15, further comprising forming a drain metal

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contact layer on a back surface of the N+ silicon substrate.

1	17. The method of claim 15, wherein the polysilicon plate comprises a
2	portion extending toward one of the DMOS trenches disposed closest to the polysilicon plate.
1	18. A trench DMOS device having a termination structure, the trench
2	DMOS device comprising:
3	a trenched DMOS device including an N+ silicon substrate, an N- epitaxial
4	layer on the N+ silicon substrate, a termination oxide layer on the N- epitaxial layer, a P body
5	in the N- epitaxial layer, a plurality of DMOS trenches extending through the P body into the
6	N-epitaxial layer, and a gate oxide layer over exposed surfaces of the P body, a plurality of
7	polysilicon gates disposed in the DMOS trenches, and a polysilicon plate disposed over the
8	termination oxide layer and over a portion of the gate oxide layer disposed adjacent the
9	termination oxide layer;
10	a plurality of N+ diffused regions formed in a portion of the P body not
11	covered by the polysilicon plate and termination oxide layer;
12	an isolation layer formed over exposed surfaces after implanting the N-type
13	ions, the isolation layer including a plurality of body contact windows extending through the
14	isolation layer and the gate oxide layer over the N+ diffused regions, and a first contact
15	window extending through the isolation layer over the polysilicon plate;
16	a plurality of P+ diffused regions formed in the N+ diffused regions at the
17	body contact windows; and
18	a source metal contact layer disposed over the isolation layer, and filling the
19	body contact windows and the first contact window.
1	19. The trench DMOS device of claim 18, further comprising a drain metal
2	contact layer on a back surface of the N+ silicon substrate.
1	20. The trench DMOS device of claim 18, wherein the polysilicon plate
2	comprises a portion extending toward one of the DMOS trenches disposed closest to the
3	polysilicon plate.
1	21. The trench DMOS device of claim 18, wherein the isolation layer
2	comprises doped silicate glass.
1	22. The trench DMOS device of claim 18, wherein the source metal
2	contact layer comprises a stack of Ti, TiN, and AlSiCu alloy layers.

1	23. A method of forming a trenched DMOS device and a termination
2	structure thereof simultaneously, the method comprising:
3	providing a silicon substrate with an epitaxial layer formed thereon, and a
4	body region defined by doping the epitaxial layer;
5	selectively etching the body region to form a plurality of DMOS trenches
6	therein;
7	forming a gate oxide layer over exposed surfaces in the body region and a
8	termination oxide layer to cover the body region;
9	depositing a polysilicon layer over exposed surfaces;
10	selectively etch the polysilicon layer to form a plurality of polysilicon gates in
11	the DMOS trenches and a polysilicon plate having an extending portion toward the body
12	region over the termination oxide layer;
13	forming sources in the body region by using the polysilicon plate as a mask;
14	and
15	forming an isolation layer and then a source metal contact layer over exposed
16	surfaces, the isolation layer protecting the polysilicon gates, the source metal contact layer
17	grounding the body region and the polysilicon plate.